CLAIMS

What is claimed is:

1. A reduced-switching multiplier circuit comprising:

a first sub-circuit; and

a second sub-circuit coupled to the first sub-circuit, the second sub-circuit receiving an input signal, the second sub-circuit outputting the input signal to the first sub-circuit when the input signal may be relevant to a next output of the first sub-circuit, and the second sub-circuit outputting a previous second sub-circuit output signal to the first sub-circuit when the input signal will not be relevant to the next output of the first sub-circuit.

2. The reduced-switching multiplier circuit of claim 1, wherein the second sub-circuit comprises:

an output circuit; and

a logic circuit controllably coupled to the output circuit, the logic circuit having a first output state when the input signal may be relevant to the next output of the first sub-circuit, and the logic circuit having a second output state when the input signal will not be relevant to the next output of the first sub-circuit.

3. The reduced-switching multiplier circuit of claim 2, wherein an output of the output circuit is coupled to an input of the output circuit.

4. The reduced-switching multiplier circuit of claim 1, wherein the second sub-circuit comprises a multiplexer, a first input of the multiplexer coupled to an output of the multiplexer, and a second input of the multiplexer coupled to the input signal.

5. The reduced-switching multiplier circuit of claim 1, wherein the second sub-circuit comprises:

a multiplexer having a first input, a second input, a select input and an output, the multiplexer output coupled to the multiplexer first input, and the multiplexer second input coupled to the input signal; and

a logic circuit having an input and an output, the logic circuit input coupled to the input signal, and the logic circuit output coupled to the multiplexer select input.

6. The reduced-switching multiplier circuit of claim 5, wherein the second sub-circuit further comprises a memory sub-circuit, an input of the memory sub-circuit coupled to the multiplexer output, and an output of the memory sub-circuit coupled to the multiplexer first input.

7. The reduced-switching multiplier circuit of claim 1, wherein the first sub-circuit comprises:

a magnitude-zeroing sub-circuit having a zero output in response to a zeroing signal; and

a sign-zeroing sub-circuit having a zero output in response to the zeroing signal.

8. The reduced-switching multiplier circuit of claim 5, wherein the logic circuit output comprises a zeroing signal output to the first sub-circuit, and wherein the first sub-circuit comprises:

a magnitude-zeroing sub-circuit having a zero output in response to the zeroing signal; and

a sign-zeroing sub-circuit having a zero output in response to the zeroing signal.

9. The reduced-switching multiplier circuit of claim 1, wherein the first sub-circuit and second sub-circuit are implemented on a single integrated circuit.

10. A method for reducing unnecessary switching in a subsequent digital circuit, the method comprising:

outputting a current output signal to the subsequent digital circuit;

receiving a next input signal;

determining, based on anticipated behavior of the subsequent digital circuit, whether the next input signal may be relevant to a next output of the subsequent digital circuit;

if the next input signal may be relevant to the next output of the subsequent digital circuit, outputting the next input signal to the subsequent digital circuit; and

if the next input signal will not be relevant to the next output of the subsequent digital circuit, outputting the current output signal to the subsequent digital circuit.

11. The method of claim 10, wherein:

the determining step comprises implementing the determining step with a digital circuit; and

the outputting the current signal step comprises coupling the current output signal from the digital circuit to an input of the digital circuit.

12. The method of claim 10, wherein the determining step comprises determining if a signal other than the next input signal will cause the next output of the subsequent digital circuit to be zero.

13. The method of claim 10, wherein the determining step comprises determining if a current state of the subsequent digital circuit will cause the next output of the subsequent digital circuit to be zero.

14. The method of claim 10, wherein the steps of the method are performed by circuitry in a single integrated circuit.

15. A switching-reduction circuit for reducing unnecessary switching in a subsequent digital signal processing circuit (SDSPC), the switching-reduction circuit comprising:

a first sub-circuit outputting a current output signal to the SDSPC;

a second sub-circuit receiving a next input signal, the second sub-circuit determining, based on anticipated behavior of the SDSPC, whether the next input signal may be relevant

to a next output of the SDSPC, the second sub-circuit causing the first sub-circuit to output the next input signal to the SDSPC when the next input signal may be relevant to the next output of the SDSPC, and the second sub-circuit causing the first sub-circuit to output the current output signal to the SDSPC when the next input signal will not be relevant to the next output of the SDSPC.

16. The switching-reduction circuit of claim 15, wherein an output of the first sub-circuit is coupled to an input of the first sub-circuit.

17. The switching-reduction circuit of claim 15, wherein the first sub-circuit comprises a multiplexer having a first input and an output, the multiplexer output coupled to the multiplexer first input.

18. The switching-reduction circuit of claim 15, wherein the first sub-circuit comprises:

a multiplexer comprising a first input, a second input, and an output; and

a memory circuit comprising a memory input coupled to the multiplexer output and a memory output coupled to the multiplexer first input.

19. The switching-reduction circuit of claim 18, wherein the multiplexer further comprises an input-select input coupled to an output of the second sub-circuit.

20. The switching-reduction circuit of claim 15, wherein the first sub-circuit and second sub-circuit are implemented on a single integrated circuit.

21. A finite impulse response filter comprising:

a plurality of taps, each having a respective multiplier circuit; and

a precoder circuit providing a current coded signal to the plurality of respective multiplier circuits, the precoder circuit comprising:

a logic circuit that receives a next input signal and forms a next coded signal in response to the next input signal, the logic circuit having a first output state when

the next coded signal may be relevant to next outputs of the plurality of multiplier circuits, and the logic circuit having a second output state when the next coded signal will not be relevant to the next outputs of the plurality of multiplier circuits; and

an output circuit coupled to the logic circuit, the output circuit outputting the next coded signal to the plurality of multiplier circuits in response to the logic circuit having the first output state, and the output circuit outputting the current coded signal to the plurality of multiplier circuits in response to the logic circuit having the second output state.

22. The finite impulse response filter of claim 21, wherein an output of the output circuit is coupled to an input of the output circuit.

23. The finite impulse response filter of claim 21, wherein the output circuit comprises a memory device having a memory input coupled to an output of the output circuit, and a memory output coupled to an input of the output circuit.

24. The finite impulse response filter of claim 21, wherein the output circuit comprises a multiplexer comprising:

a first multiplexer input coupled to the next coded signal; and

a second multiplexer input coupled to the current coded signal.

25. The finite impulse response filter of claim 21, wherein the output circuit comprises a multiplexer comprising:

a multiplexer output;

a first multiplexer input coupled to the next coded signal;

a second multiplexer input coupled to the multiplexer output; and

a select input coupled to the logic circuit.

26. The finite impulse response filter of claim 25, wherein the output circuit further comprises a memory device having a memory input coupled to the multiplexer output, and a memory output coupled to the second multiplexer input.

27. The finite impulse response filter of claim 21, wherein at least one of the multiplier circuits comprises:

a magnitude-zeroing sub-circuit having a zero magnitude output in response to the logic circuit having the second output state; and

a sign-zeroing sub-circuit having a zero sign output in response to the logic circuit having the second output state.

28. The finite impulse response filter of claim 21, wherein the precoder circuit is implemented on an integrated circuit.

29. A method for reducing power consumption in a Booth-type multiplier circuit having a pre-coder stage and a multiplier stage, the method comprising:

determining if the next input to the multiplier stage from the pre-coder stage will include a zeroing signal to zero the magnitude output of the multiplier stage; and

if the next input to the multiplier circuit will include a zeroing signal to zero the magnitude output of the multiplier stage, outputting the zeroing signal to the multiplier stage and maintaining at least one other input signal to the multiplier stage at its current value.

30. The method of claim 29, further comprising setting a sign bit output from the multiplier stage to a zero value if the next input to the multiplier stage includes the zeroing signal.